

Project Proposal Ellis Ashton

by Ellis Ashton

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BEng Electrical and Electronic Engineering

Independent Project (ACCA6020)



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Research Proposal

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1. Introduction

The ability to diagnose and correct electrical faults is fundamental to an electrical engineering education. Traditional teaching methods often involve static demonstration circuits or theoretical exercises, which limit students' exposure to realistic fault scenarios. This project proposes the development of a microcontroller-based electrical fault simulator that can electronically generate a variety of circuit fault conditions for educational use. The simulator will enable inexperienced students to develop diagnostic skills in a safe, controlled environment without requiring manual component reconfiguration.

This project will improve the accessibility into electrical commissioning and test for students of all backgrounds but providing a visual learning tool that can overcome ethnicity and/or language barriers for students. Simulation is being introduced in many aspects of training from classrooms to military applications, this use of embedded systems helps to streamline and focus teaching delivery.

2. Literature review and project background

The project builds upon emerging trends in embedded systems and digital fault simulation, where microcontrollers are increasingly used to replicate physical circuit behaviours [1]. Research shows that experiential learning through controlled fault testing significantly enhances problem-solving skills and confidence in students [2]. Fault simulation systems have been implemented in automotive diagnostics [3], power distribution training [4], and industrial safety laboratories [5], but educational institutions continue to face barriers such as high costs, limited configurability, and safety concerns with existing equipment.

Studies by Ahmed et al. [6] and Chen et al. [7] demonstrate that programmable fault injection improves learner understanding of circuit behaviour and troubleshooting processes. Similarly, embedded-based diagnostic trainers allow for fault conditions such as open circuits, short circuits, sensor malfunctions, and resistive faults to be introduced dynamically through software control. However, these systems are often proprietary, expensive, and unsuitable for basic educational laboratories [8].

This creates a clear research and implementation gap in the availability of low-cost, modular, and scalable fault simulation systems designed specifically for training environments. Therefore, this project seeks to create a cost-effective educational tool that integrates both hardware and firmware control for introducing predefined electrical faults, with the added goal of reducing maintenance requirements and improving safety compliance.

2.1 Problem Statement

There is a lack of affordable, modular, and safe educational tools that allow students to practice electrical fault diagnosis under realistic and varied conditions. Existing solutions are often cost-prohibitive, lack adaptability, or require manual configuration that increases wear and safety risk. Many of the existing systems are based around large control circuits whereas this project will provide a low-cost procedural trainer that addresses the sustainability and ethical concerns surrounding the existing method of teaching. The

sustainability and ethical shortfalls in current teaching practices that have been identified include waste, maintenance and procedural teaching that is applicable across different systems.

2.2 Aim

To design, develop, and evaluate a microcontroller-based electrical fault simulator that allows users to identify, test, and diagnose various circuit fault conditions in a safe and controlled educational environment. The product should be capable of switching between faults with no additional hardware configuration required, allowing the control circuit to be contained. This increases the safety of the system by only giving the students physical access to the dedicated testing points.

2.3 Objectives

1. To review current electrical fault simulation technologies and educational training systems that are available, with particular focus to directly competing products.
2. To design an embedded system capable of introducing multiple fault types using microcontroller-controlled switching, without needing any physical reconfiguration.³
3. To develop the simulator hardware, firmware, and user interface for fault selection and system control that will support at least 4 simulated fault conditions.⁴
4. To evaluate system performance, usability, and educational effectiveness through testing and user feedback.

2.4 Expected Outcomes

The project will deliver a functional prototype of the electrical fault simulator, complete with control firmware, circuit schematics, and documentation. The system will provide reproducible fault scenarios, configurable through buttons or a digital interface, and can be integrated into laboratory exercises for student use.

3. Project Design



The project will adopt a product development approach, focusing on the creation and evaluation of a functional prototype. The system will use a PIC microcontroller as the central controller, managing relays or transistor switches that electronically introduce specific circuit faults. Users (students) will select different fault scenarios via push-buttons or an LCD menu interface, with the results observable at test points and indicators on the simulator board.

Example fault conditions to be implemented include open circuits, short circuits, resistive faults, and ground faults.  conditions will be controlled programmatically without requiring physical rewiring, ensuring rapid testing and safe operation. There will be an assessment of the faults that can be added within the given timescale, the project will serve to provide an iteration of the design that could be further developed to include additional faults outside of this project timescale.

The hardware will be designed and simulated using Proteus Design Suite, with circuit schematics developed in ISIS and PCB layouts in ARES. The control firmware will be written in C using the CCS C Compiler, consistent with established microcontroller development workflows. The project will include modular sub-systems for power regulation, microcontroller logic, fault switching, and LED/LCD feedback. The system will undergo testing that will determine the later scalability and compatibility with growth requirements.

Firmware development will follow an iterative design methodology involving prototyping, debugging, and refinement through testing. This method will allow for product development whilst allowing the product to remain operational between iterations, further development iterations can be carried out outside of the given timescale.

Data collection will focus on system performance, user evaluation, and reliability testing. Quantitative data such as timing and voltage readings will be analysed statistically, while qualitative user feedback will be evaluated using thematic analysis. This will include the surveying of both students and lecturers/industrial personnel to assess the market demand for the product.

A structured risk assessment will identify potential hazards such as electrical risks, component failure, software malfunction and scheduling delays. Mitigation will include low-voltage operation, circuit protection, extensive testing, and progress tracking. Further mitigations will be considered as the project develops and testing highlights areas that require additional safety controls and further development.

Ethical considerations include voluntary and anonymous user participation during testing, with no personal data collected. The feedback will be processed in an anonymous method to ensure that no personal data is held or processed.

Sustainability will be addressed through low-power design, reusable components, and long-term reusability, supporting reduced waste and maintenance. Data analysis will employ descriptive statistics and qualitative evaluation to assess accuracy, repeatability, and effectiveness of the system. The system being reusable in comparison with the current method within colleges and learning institutions where cable and components are wasted in the process of demonstrating faults, allows this replacement solution to provide a more sustainable method of providing the learning service.

4. Resources and Planning

Hardware: PIC18F4550 microcontroller, relays or MOSFETs, resistors, LEDs, switches, LCD display, and power modules.

Software: Proteus Design Suite (ISIS/ARES), CCS C Compiler, MPLAB X IDE.

Laboratory Equipment: Multimeter, oscilloscope, power supply, and test leads.

Many of the above-mentioned resources are available at the University, if the components/resources are not available then they will be ethically procured where alternatives can't be sourced.

Expected timeline:

Weeks 1–2: Literature review and concept validation.

Weeks 3–4: System design (hardware and firmware architecture).

Weeks 5–7: Circuit simulation and prototype testing.

Weeks 8–10: Hardware implementation and firmware testing.

Weeks 11–12: System evaluation and data collection.

Weeks 13–14: Final report writing and presentation preparation.

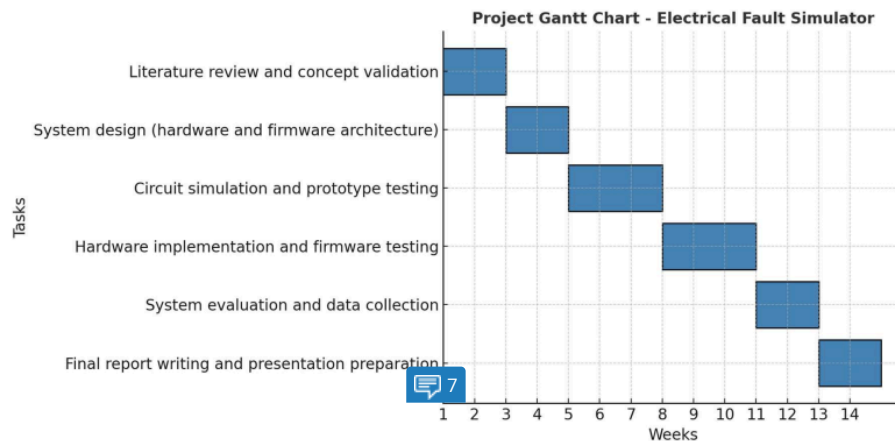


Figure 1 Gantt chart

5. Expected Deliverables

1. Fully functional electrical fault simulator prototype.
2. Circuit schematics, PCB layout, and firmware documentation.
3. Test and evaluation report summarising performance.
4. Final project report with discussion of sustainability and safety.

This prototype will be used for further development where information and feedback will be used to improve the product by increasing liability and addressing any other concerns that are highlighted during the testing phase. Once the system is in use, feedback gathered will also focus on the possibility of introducing additional fault simulation capability to improve the systems application.

As live voltages are being used, the system will be tested extensively to ensure that any safety controls are in place. The use-case for the product will include being supervised by a competent person with suitable electrical training to ensure that the product is being used in a safe manner. However, if this product can be developed and refined suitably so that students can use this unsupervised with minimal risk, then suitable controls will be outlined during testing. The testing of this system will include reliability and safety tests to ensure that the system is safe for inexperienced students.

In conclusion, this proposal outlines the development of a cost-effective and sustainable electrical fault simulator that promotes safety, inclusivity, and skill development in electrical engineering education. By combining embedded systems design with ethical and sustainable principles, the project aims to provide a scalable educational tool that enhances both teaching and learning outcomes.

References

- [1] S. K. Ahmed, "Embedded Fault Simulation Techniques in Electrical Education," *IEEE Trans. Educ.*, vol. 66, no. 3, pp. 412–420, 2023.
- [2] M. Chen and L. Zhang, "Microcontroller-Based Diagnostic Systems for Technical Training," *Int. J. Eng. Pedagogy*, vol. 11, no. 2, pp. 45–56, 2022.
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- [8] D. F. Zhao, "Low-Cost Embedded Teaching Systems for Electrical Training," *Int. J. Innov. Eng. Educ.*, vol. 10, no. 2, pp. 102–110, 2021.

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GRADEMARK REPORT

FINAL GRADE

70/100

GENERAL COMMENTS

Project Proposal – ACCA6020 Independent Project

Student: Ellis Ashton

Intro / Aims & Objectives: 16/20

The introduction is clear, and the aims and objectives presented. The Objectives section could be improved noting the hardware/firmware, fault-selection method interface, and evaluation approach.

Clear, but could be enhanced with brief objective details.

Background to the Project / Literature Review : 14/20

The background provides a strong overview of existing and clearly highlights the need for a low-cost, configurable simulation tool. However, it could be improved by briefly clarifying how current limitations justify the proposed solution.

Requires clearer reasoning.

Project Design : 21/30

The project design is well structured and provides a good overview of the simulator's hardware, firmware, and software. However, the description does not sufficiently explain how the simulator connects to the actual circuit being tested, how the system identifies or monitors the injected faults. Including a block diagram would also help to understand how faults are injected and observed.

Adding details about the physical test interface, measurement points, fault-detection method, and how users interact with the real circuit will strengthen the technical clarity.

Resources / Planning :8/15

The Gantt chart shows a clear outline, but it needs additional details such as integration milestones, contingency time for hardware procurement, and preparation for testing and presentation to fully cover a project running until the end of the Project. (could be redrawn referring this 'Specific milestones: hardware procurement, hardware assembly stages, integration phases, testing phases, validation phase, parallel tasks).

allowance/buffer time, contingency time, preparation testing, preparation for final presentation.')

More detailed and complete clearer milestones for better coverage of all project stages.

Document Presentation:11/15

The project title is missing. The document is otherwise presented, with good structure, readability, and neat organisation. The overall presentation could be improved by strengthening the project planning section and adding in the Project Design chapter.

Neat presentation!

TOTAL:70/100

PAGE 1



Comment 1

Title of the Project is missing.

PAGE 2

PAGE 3

PAGE 4

PAGE 5



Comment 2

Clarify how the proposed system's features directly address this gap.

PAGE 6



Comment 3

Any Particular type?



Comment 4

names of them could be addressed here instead of generally writing.



Comment 5

Adding details about the physical test interface, measurement points, fault-detection method, and how users interact with the real circuit will strengthen the technical clarity of this chapter.



Comment 6

To give more clarity, it could be better if some visual aids such as block diagrams are added.



Comment 7

It would be beneficial to develop a broader and clearer Gantt chart that includes specific milestones, hardware procurement and assembly stages, integration and testing phases, a validation phase, parallel tasks where appropriate, risk-allowance or buffer time, contingency time, and preparation for user testing and the final presentation.